REMARKS

Claims 1, 3-17 and 19-22 are pending in the above-identified application. The following objections and rejections are respectfully traversed in light of the following remarks, and reconsideration is requested.

Claims 1, 3-17 and 19-22 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the rejection, the Examiner stated:

> Scope of Claim 1 is not clear. The claim fails to recite functional relationship between the register file, the decoder and the functional unit. It is not clear how the register file and the functional unit are related to deriving register spedifier [sic] by the decoder. The functional unit and the register file as recited are neither helping the decoder to derive specifier nor using the derived specifier.
>
> In claim 4, there is no functional relationship between the components of claim 4 and parent claim 1. The term 'said' should be used if claim 4 further limits the components of parent claim 1. Other claims have similar defect. See the decoder in claim 17 for example.
>
> In claim 7, it is not clear how the recitation in lines 5-8 is related to control transfer.
>
> With respect to claim 19, it is not clear what is meant by 'the register file generating two pointers'. Note that a register file is for storing or outputting operands in response to register specifiers. A register file does not generate pointers.
>
> Further with respect to claim 1, 3-16, there is nothing recited in the claims to execute instructions in a manner as recited in dependent claims 3-16.
>
> Scope of limitation of the following is not clear:
>
> 1. 'the instruction in which a register specifier is implicitly derived' in line 5 of claim 1. Note that an instruction

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> by itself can not derive anything. An instruction is nothing more than a command.
>
> 2. 'the processor is a Very Long Instruction Word' in claim 4. A processor is not a word.

In response, Applicants respectfully contend that the above rejection is improper as the Examiner fails to state the basis for the rejections with clearness and particularity. The Examiner's statement that "there is nothing recited in the claims to execute instructions in a manner as recited in dependent claims 3-16" is ambiguous at best. The Examiner appears to reject Claim 1 on the basis that the claim is not detailed enough for the Examiner. A claim may not be subject to rejection under 35 USC 112, second paragraph, merely because it is broad. See MPEP 2173.04. Claim 1 clearly recites the structural relationship between a register file, a functional unit and a decoder and recites the functions of the functional unit and the decoder which act upon the register file. MPEP 2173.04 [Breadth Is Not Indefiniteness] states that:

> Breadth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different form that defined in the claims, then the claims comply with 35 USC 112, second paragraph.

Though broad, the scope of the subject matter embraced by Claim 1 is clear. The title of the application is "Implicitly Derived Register Specifiers In A Processor" and Claim 1 clearly states the elements of Claim 1 cooperate such that an explicitly-specified register specifier of an instruction is used to implicitly derive another register specifier. Claim 1 is replete with structural and functional relationships.

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Claim 4 has been amended to state the relationship between the registers and the register file segments. Claim 4 has been amended to clarify that the processor is a VLIW processor. No new matter is added. Claim 17 has been amended in light of the incorporation of Claim 2 into Claim 1. With respect to Claim 7, lines 5-8 describe where the address of an instruction word (i.e., the instruction word that follows the instruction word begun with the call instruction) is held; this address is an implicit operand of the call instruction (Specification, page 24, line 23 to page 25, line 9). With respect to Claim 19, the meaning of the claim is clear in light of the specification. While limitations in the specification are not read into the claims, the claims are interpreted in light of the specification.

Therefore, in view of the foregoing, it is respectfully requested that the Examiner withdraw the rejections to Claims 1, 3-17 and 19-22 under 35 USC 112, second paragraph.

Claims 1, 3-17 and 19-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tannenbaum (textbook) in view of Fleck. In the rejection, the Examiner stated:

> Figure 3-17 of Tannebaum shows numerous format that an instruction can have. Figure 3-16 shows an instruction having having [sic] 4 fields, namely, an opcode field and 3 address or operand fields. Each of the addres [sic] fields contains an address of an operand stored in a register or in a memory location. The opcode field contains an operation of any types to be performed on two of the operands and the result is stored in the third operand address. From Figure 3-16, it is clear that an instruction having fields containing operand addresses and opcodes is well-known in the art. It is further well known that opcodes can be of any type, for examples, combination of multiplication, division, subtraction or addition on operands represented by integer, floating point of single or double precision (see section 3.3 ADDRESSING, page 79-80).
>
> The operand addresses shown in Figure 3-16 are explicit address. The drawing does not show deriving implicit address from explicit address. The technique is called "indexing" or "autoindexing" which is taught in section 3.3.5 INDEXING (page 84-85) of Tannenbaum. The section also discloses that indexing is used in IBM 370 and PDP11.

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> Tannenbaum fails to show that IBM 370 or PDP11 or any computer having basic components such as register file, decoder, and functional unit. However, Fleck taught that, as admitted by applicants, register file, decoder and functional units are basic components of a computer. From the teaching of Tannenbaum and Fleck, it would have been obvious to a person of ordinary skill in the art to implement indexing on a computer having register file, decoder and functional unit having any types of instruction sets.

Applicants respectfully traverse the Examiner's rejections of Claims 1, 3-17 and 19-22. The Examiner's rejections are ambiguous at best. It is not clear whether the Examiner is asserting Fleck in combination with Tannenbaum or as a reference to support that something is well-known in the art. The Examiner fails to point out and distinctly state where specifically the Applicants allegedly admitted that 'register file, decoder and functional units are basic components of a computer'. The Examiner's use of a generic textbook and unsupported position cannot ease the Examiner's required burden of proof in demonstrating that all elements of the claims are disclosed in the reference. See MPEP 706.02(j). By the Examiner's own admission, Tannenbaum does not disclose all the elements of the claims, namely 'deriving [an] implicit address from [an] explicit address' and 'any computer having basic components'. Additionally, the Examiner confuses the technique of "deriving an implicit address from an explicit address" with the technique called "indexing" or "autoindexing"; these are two different techniques. The prior art must disclose the teaching or suggestion to make the claimed combination and a reasonable expectation of success. Tannenbaum does not disclose any teaching or suggestion to make the claimed combination.

The Examiner fails to meet the requirements of MPEP 706.02(j) [Contents of a 35 USC 103 Rejection] which states:

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> 35 USC 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references....
>
> .... Finally, the prior art reference (or references when combined) must teach or suggest *all claim limitations*. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143-2143.03 for decisions pertinent to each of these criteria.
>
> ...*The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done*. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Capp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). [Emphasis added.]

The Examiner has based the rejections of Claims 1, 3-17 and 19-22 on the position that somehow Tannenbaum teaches the claimed invention. However, the Examiner has failed to show that Tannenbaum in view of Fleck teaches or suggests all claim limitations. The Examiner discusses the claims in only the most generic manner. The Examiner fails to point out that Tannenbaum does not teach VLIW. In fact, Tannenbaum teaches away from VLIW and explicitly states "[f]irst, and most important, short instructions are better than long instructions." (Tannenbaum, page 71, section 3.2.1). Therefore, Applicants respectfully request reconsideration and withdrawal of the rejections to Claims 1, 3-17 and 19-22 under 35 U.S.C. § 103(a).

Claims 1, 3-17 and 19-22 are provisionally rejected under the judicially created doctrine of double patenting over claims 1-29 of copending Application No. 09/204,585 in view of Tanenbaum. In the rejection, the Examiner stated:

> The claims of 09/204,585 recites [sic] a plurality of functional units, a decoder and a register. The claims do not state how addresses of register file are formulated. However,

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> Figure 3-16 of Tannenbaum teaches how register addresses are implicitly derived from explicit addresses. Since both references are directed toward addressing register file, it would have been obvious to a person of ordinary skill in the art to formulate register addresses as taught by Tannenbaum so that address field in an instruction can be shorter.
>
> Applicant's [sic] arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Applicants recognize the provisional nature of the rejections, and will address the need for a terminal disclaimer or other course of action in future communications to this Office should Claims 1-29 of copending Application No. 09/204,585 be allowed at some future point in time and in the same, or substantially the same, form as they now presently exist. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejections to Claims 1, 3-17 and 19-22 under the judicially created doctrine of double patenting.

CONCLUSION

For the foregoing reasons, Applicant believes the pending Claims 1, 3-17 & 19-22 are allowable, and a Notice of Allowance is respectfully requested. The Examiner is invited to call the Applicants' Attorney at (949) 718-5200 for any questions with this response.

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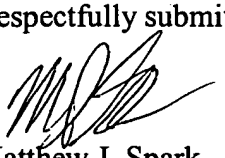
Respectfully submitted,



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ATTACHMENT A

This response amends Claims 1, 4 & 17 as follows.

1. (Twice Amended) A processor comprising:

a register file including a plurality of registers;

a functional unit, coupled to the register file, [the functional unit that executes] executing an instruction operating upon [a] said plurality of registers in the register file, the instruction in which a register specifier is implicitly derived, based on [another] an explicitly-specified register specifier; and

a decoder coupled to the functional unit and coupled to the register file, the decoder implicitly deriving [a] said implicitly derived register specifier based on [an] said explicitly-specified register specifier of the instruction.

4. (Amended) A processor according to Claim 1 wherein the processor is a Very Long Instruction Word (VLIW) processor and [further comprising:] wherein

[a] said register file further including a plurality of register file segments wherein the plurality of registers are divided among said plurality of register file segments; and

wherein said VLIW processor further comprises a plurality of functional units, ones of the plurality of functional units being coupled to and associated with respective ones of the register file segments.

17. (Amended) A processor according to Claim 1, [further comprising:

a decoder coupled to the functional unit and coupled to the register file, the decoder implicitly deriving a register specifier based on an explicitly-specified register specifier of the instruction and] wherein said decoder is generating a first pointer to the explicitly-specified register and a second pointer to the implicitly-derived register.

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